

A4  
LSI design. Ultimately, the LSI design foundry prepares the netlist using this scan FF d2403. Thereafter, the netlist d2403 is passed to the client of LSI design.

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IN THE CLAIMS:

Please cancel Claims 2-16 without prejudice or disclaimer.

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A5  
1           1. (Amended) A storage circuit comprising:  
2           a first logic gate for receiving a first signal and a  
3           second signal, and for selectively outputting either the  
4           first signal or the second signal in accordance with a  
5           control signal;  
6           a first storage element for receiving a clock signal,  
7           for storing an output signal of the first logic gate in  
8           response to the clock signal, and for outputting the stored  
9           signal as a third signal in response to the clock signal;  
10          and  
11          a second logic gate for receiving the third signal  
12          from the first storage element, said second logic gate  
13          fixing an output signal thereof, regardless of the received  
14          third signal, in response to the control signal;

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15 wherein the storage circuit, having a first output and  
16 a second output, outputs the third signal through the first  
17 output, and the output signal of the second logic gate  
18 through the second output.

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Please add the following claims:

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1 17. (New) A storage circuit having first and second  
2 outputs, comprising:  
3 a first logic gate for receiving a first signal and a  
4 second signal, and for selectively outputting either the  
5 first signal or the second signal in accordance with a  
6 control signal;  
7 a first storage element, having a master latch and a  
8 slave latch, wherein the master latch inputs an output  
9 signal of the first logic gate and latches the output  
10 signal of the first logic gate in response to the clock  
11 signal, and the slave latch inputs an output signal of the  
12 master latch and passes the output signal of the master  
13 latch to the first output of the storage circuit in  
14 response to an inverted clock signal;  
15 a second logic gate for receiving the output signal of  
16 the master latch, and for outputting the output signal of

17 the master latch to the second output of the storage  
18 circuit in response to the control signal.

1 18. (New) A storage circuit comprising:  
2 a first logic gate for receiving a first signal and a  
3 second signal, and for selectively outputting either the  
4 first signal or the second signal in accordance with a  
5 first control signal;  
6 a first storage element for receiving a clock signal,  
7 for storing an output signal of the first logic gate in  
8 response to the clock signal, and for outputting the stored  
9 signal as a third signal in response to the clock signal;  
10 and  
11 a second logic gate for receiving the third signal  
12 from the first storage element, said second logic gate  
13 fixing an output signal thereof, regardless of the received  
14 third signal, in response to a second control signal,  
15 wherein the storage circuit, having a first output and  
16 a second output, outputs the third signal through the first  
17 output, and the output signal of the second logic gate  
18 through the second output.

1 19. (New) A storage circuit according to claim 18,

Ag 2 wherein the second control signal is fixed to a low  
3 level earlier than the first control signal at a time of a  
4 transition from a scan-in operation to a logic test  
5 operation.

1 20. (New) A semiconductor integrated circuit  
2 comprising:

3 a first storage circuit including first and second  
4 input terminals, first and second output terminals, a first  
5 control terminal for receiving a control signal, first and  
6 second logic gates, and a first storage element;

7 a logic circuit for receiving an output signal of the  
8 first output terminal of the first storage circuit, for  
9 performing a predetermined processing on the output signal,  
10 and for outputting a result of the processing; and

11 a second storage circuit including third and fourth  
12 input terminals, and a second control terminal for  
13 receiving the control signal,

14 wherein the first logic gate receives a first signal  
15 of the first input terminal and a second signal of the  
16 second input terminal, and selectively outputs either the  
17 first signal or the second signal in accordance with the  
18 control signal of the first control terminal;

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19 wherein the first storage element receives a clock  
20 signal, stores an output signal of the first logic gate in  
21 response to the clock signal, and outputs the stored signal  
22 by way of a third signal in response to the clock signal;

23 wherein the second logic gate receives the third  
24 signal from the first storage element, the second logic  
25 gate fixing an output signal thereof, regardless of the  
26 received third signal, in response to the control signal of  
27 the first control terminal;

28 wherein the first storage circuit outputs the third  
29 signal through the first output terminal to the logic  
30 circuit, and the output signal of the second logic gate  
31 through the second output terminal to the second storage  
32 circuit; and

33 wherein the second storage circuit receives the output  
34 signal from the first storage circuit through the third  
35 input terminal and the output signal of the logic circuit  
36 through the fourth input terminal, and selectively stores  
37 either the output signal of the logic circuit or the first  
38 storage circuit in accordance with the control signal of  
39 the second control terminal.

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